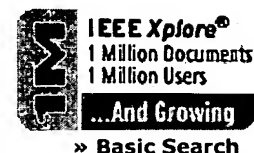


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1 Group testing with DNA chips: generating designs and decoding experiments
Schliep, A.; Torney, D.C.; Rahmann, S.;

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Pages:84 - 91

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) **IEEE CNF**
2 Conference Record of Thirty-Fifth Asilomar Conference on Signals, Systems and Computers (Cat.No.01CH37256)

Signals, Systems and Computers, 2001. Conference Record of the Thirty-Fifth Asilomar Conference on , Volume: 1 , 4-7 Nov. 2001

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3 System level design, a VHDL based approach
van den Hurk, J.; Dilling, E.;

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Pages:568 - 573

[\[Abstract\]](#) [\[PDF Full-Text \(528 KB\)\]](#) **IEEE CNF**
4 High performance, high throughput turbo/SOVA decoder design
Zhongfeng Wang; Parhi, K.K.;

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6 Probabilistic application modeling for system-level performance analysis

Marculescu, R.; Nandi, A.;

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